Minilogic Device Corporation

MLCM Series Dot Matrix LCD Module Specification

Part No.	First Edition	Final Edition	Original Date	Customer No.
MLCM8016	A	A	31/03/03	-

Table of Contents

Revisions

Date	Rev.	Modified Area				Description	Engineer Approved
		Elect.	Mech.	Pin Config.	Others.		
31/03/03	A					First Edition	Anthony Tsang

1.0 Application

- Instrument Display
- Telephone Display
- Automotive Display
- Small and Compact Handheld Device Display
- Display Message in various language
- Graphic Display
- Programmable Animation and other display effect

2.0 Features

- Standard COG (Chip on Glass) Dot Matrix LCD Module
- Standard 14 - Pins Interface.
- Slim dimension Module : thickness 22 – 85 mm.
- Welcome custom design on Dot size and other mechanical dimension.
- Welcome to add custom icons on module by installing ML1001 Static LCD COG driver.

3.0 MLCM Series Dot Matrix LCD Module General Description

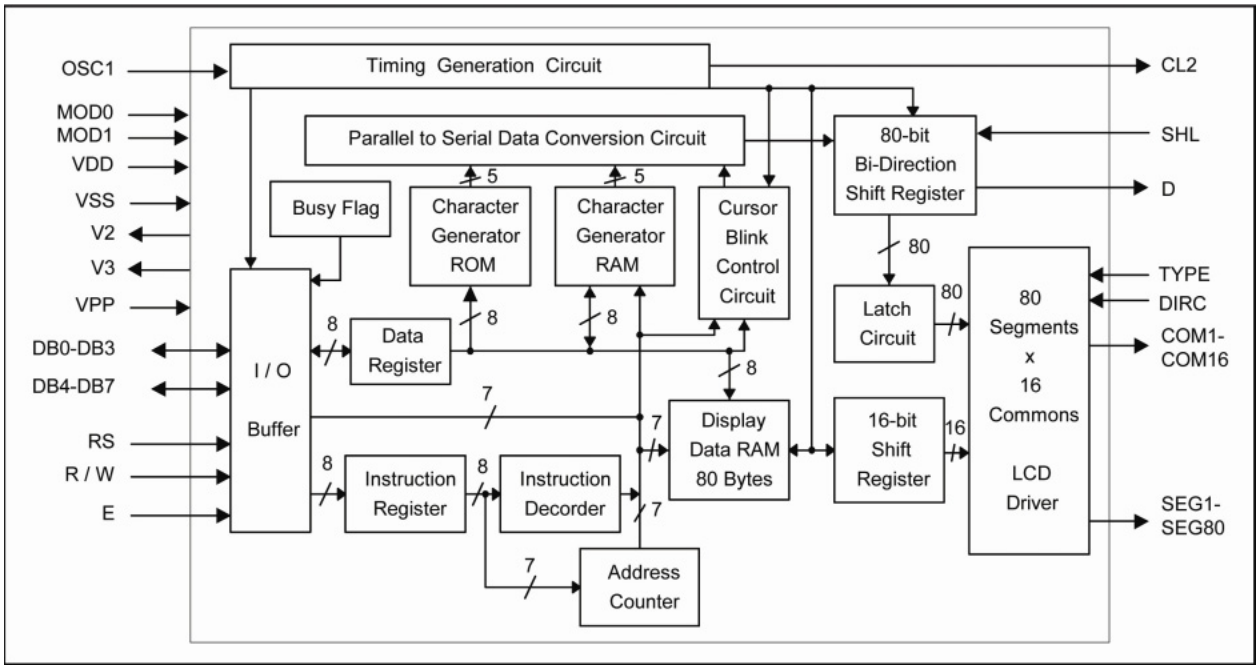
The MLCM Series Dot Matrix LCD Modules are all COG (Chip on Glass) LCD Modules. COG LCD module doesn't require any PCB and bezel. The advantages of not using PCB and bezel are:

1. If user wants to change the dimension of the LCD module, they don't need to change the design of the PCB and bezel, hence faster the time to market and spend a much cheaper tooling.
2. It would be lighter by not having plastic PCB and steel bezel.

With the use of ML1001 series driver, User can add their icons or 7 segments Digits on the LCD Module.

Apart from the standard LCD Module listed below, we welcome any kind of CUSTOM made LCD module.

4.0 MLCM8016 Block Diagram



5.0 MLCM8016 General Specification

Display Format:	16 (character) X 2 (line)
Dot size:	0.6 mm (H) X 0.6 mm (W)
Dot pitch:	0.65 mm (H) X 0.65 mm (W)
Viewing area:	15.70 mm (H) X 61.00 mm (W)
LCD Type:	STN
Polarizer:	Transflective / Reflective / Transmissive
Operating Voltage:	5.0V
Viewing angle:	6:00
Operating Temperature:	-20 to +70℃
Storage Temperature:	-30 to +80℃

6.0 Functional Descriptions

6.1 Oscillator

The built-in RC oscillator generates suitable clock for operation

6.2 Control and display instructions

6.2.1 Clear display

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the whole display and sets display data RAM's address 0 in address counter.

6.2.2 Return home

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Don't Care (0 or 1)
It sets display data RAM's address 0 in address counter and display returns to its original position. The cursor or blink goes to the left edge of the display. The content of the Display Data Ram does not change.

6.2.3 Entry mode set

During writing and reading data, it sets cursor move direction and shifts the display.

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

S = 1	I/D = 1	It shifts the display to left
S = 1	I/D = 0	It shifts the display to right

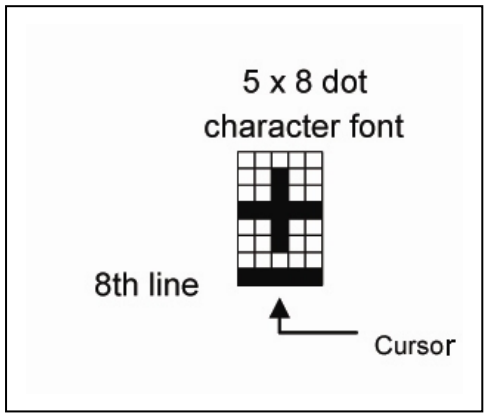
6.2.4 Display ON/OFF control

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

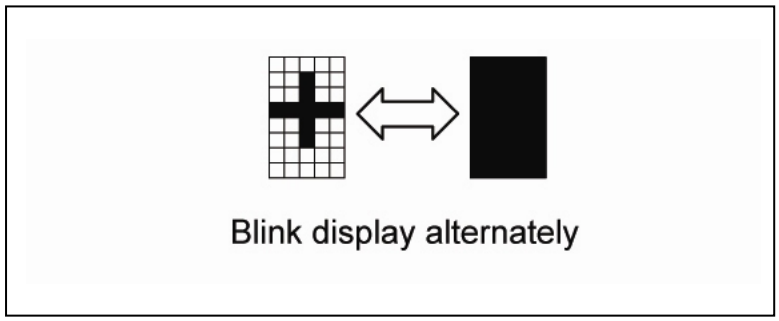
B = 1: Blinks on, B = 0: Blinks off



6.2.5 Cursor or display shift

Without changing DD RAM's data, it can move cursor and shift display.

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



S/C	R/L	Description	Address Counter
0	0	Shift cursor to left	AC = AC - 1
0	1	Shift cursor to right	AC = AC + 1
1	0	Shift display to left. Cursor follows the display shift	AC = AC
1	1	Shift display to right. Cursor follows the display shift.	AC = AC

6.2.6 Function set

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Don't Care (0 or 1)
DL: It sets interface data length
DL = 1: Data are transferred with 8-bit lengths (DB0 – DB7).
DL = 0: Data are transferred with 4-bit lengths (DB4 – DB7)
(It requires transferring data twice)
N: It sets the number of the display line.
N = 0: One-line display.
N = 1: Two-line display.
F: It sets the character font.
F = 0: 5 x 8 dots character font.
F = 1: 5 x 10 dots character font.

N	F	Display lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

Note: In this 16 character x 2 lines LCD Module, users have to choose N = 1 in this Command.

6.2.7 Set character generator RAM address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

Set character generator RAM address to AC. This instruction makes character generator RAM data available from MPU.

6.2.8 Set display data RAM address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	A	a	a	a	a	a

Set display data RAM address to AC. This instruction makes display data RAM data available from MPU. When 1-line display mode (N=0), display data RAM is from "00H" to "4FH". In

2-line display mode (N = 1), display data RAM address in the 1st line is from “00H” to “27H”, and display data RAM address in the 2nd line is from “40H” to “67H”.

6.2.9 Read busy flag and address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	a	a	a	a	a	a	a

When (BF = 1) indicates that the system is busy now; it will not accept any instruction until busy flag clears (BF = 0). At the same time, the address counter contents shall be read out.

6.2.10 Write data to character generator RAM or display data RAM

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes binary 8-bit data to character generator RAM or display data RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

6.2.11 Read data from character generator RAM or display data RAM

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads binary 8-bit data from character generator RAM or display data RAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, because the direction of AC is not determined. In case of display data RAM read operation, cursor shift instruction plays the same role as display data RAM address set instruction; it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After character generator RAM read operation, display shift may not be executed correctly.

6.3 Instruction table

Instruction	Instruction Code										Description	Execution time
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		(fosc=270KHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM and Set DDRAM address to “00H” from AC	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	38us
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	38us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	38us
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F: 5x10/5x8 dots)	38us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	38us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	38us
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write Data into internal RAM (DDRAM/CGRAM)	38us
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read Data from internal RAM (DDRAM/CGRAM)	38us

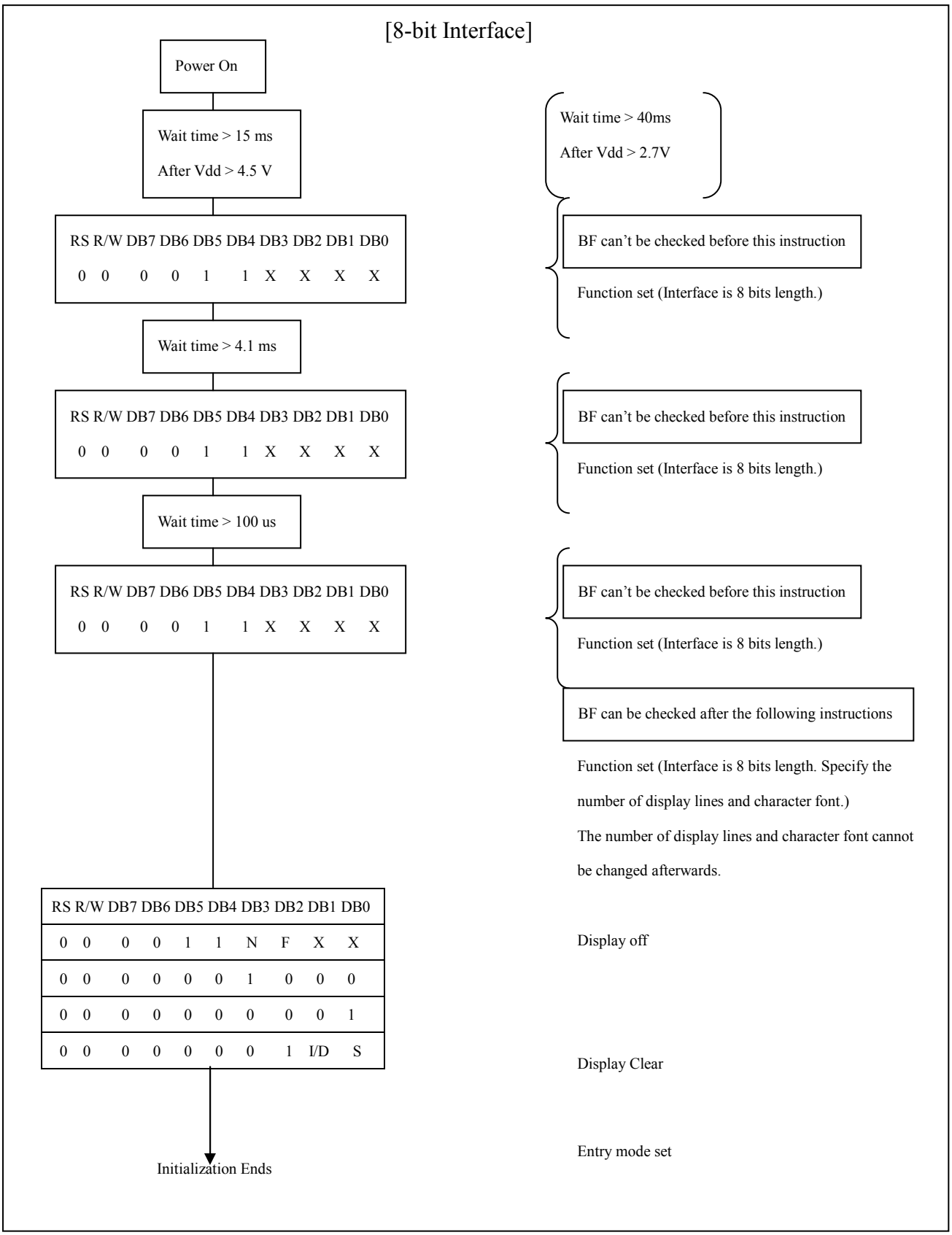
Note : “-“, don’t care

6.4 Example of 8-bit operation & 16-digit 2-line display (use internal reset)

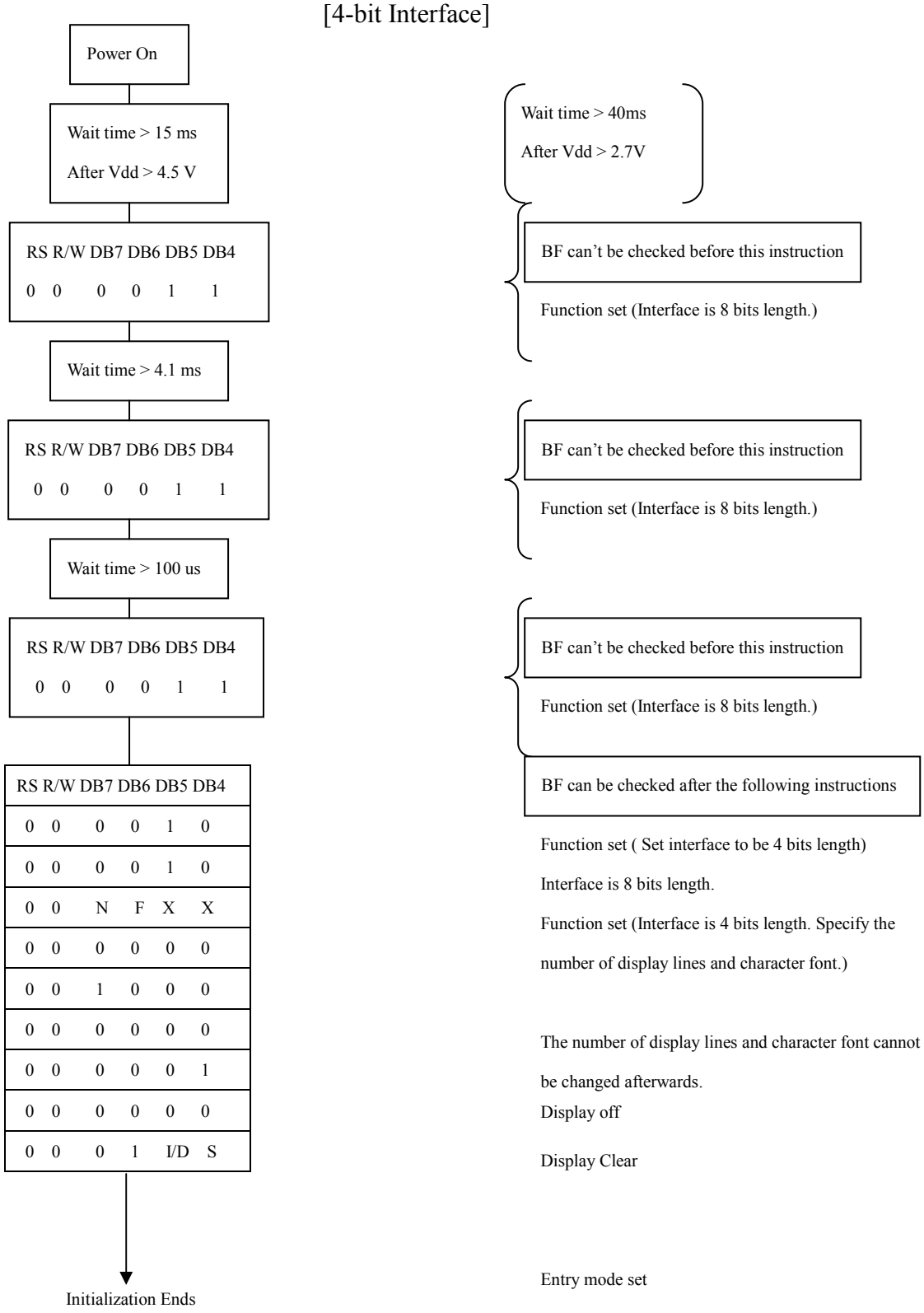
NO.	Instruction	Display	Operation
1	Power On.		Power on reset. No display.
2	Function Set RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display and 5x7 dot character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display On. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM/DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write “W”. The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write data to CG RAM/DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write “E”. The cursor is incremented by one and shifted to the right.
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DDRAM’s address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM/DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write “T”. The cursor is incremented by one and shifted to the right.
10	Write data to CG RAM/DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TOPART_	Write “T”. The cursor is incremented by one and shifted to the right.
11	Entry mode set 0 0 0 0 0 0 1 1 1 0	WELCOME TOPART_	When writing, it sets mode for the display shift.
12	Write data to CG RAM/DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME OPARTY_	Write “Y. The cursor is incremented by one and shifted to the right.
13	:	:	
14	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TOPARTY	Both the display and the cursor return to the original position (address 0).

6.5 Initialization

At power on, it starts the internal auto-reset circuit and executes the initial instructions. There are the initial procedures shown as below:

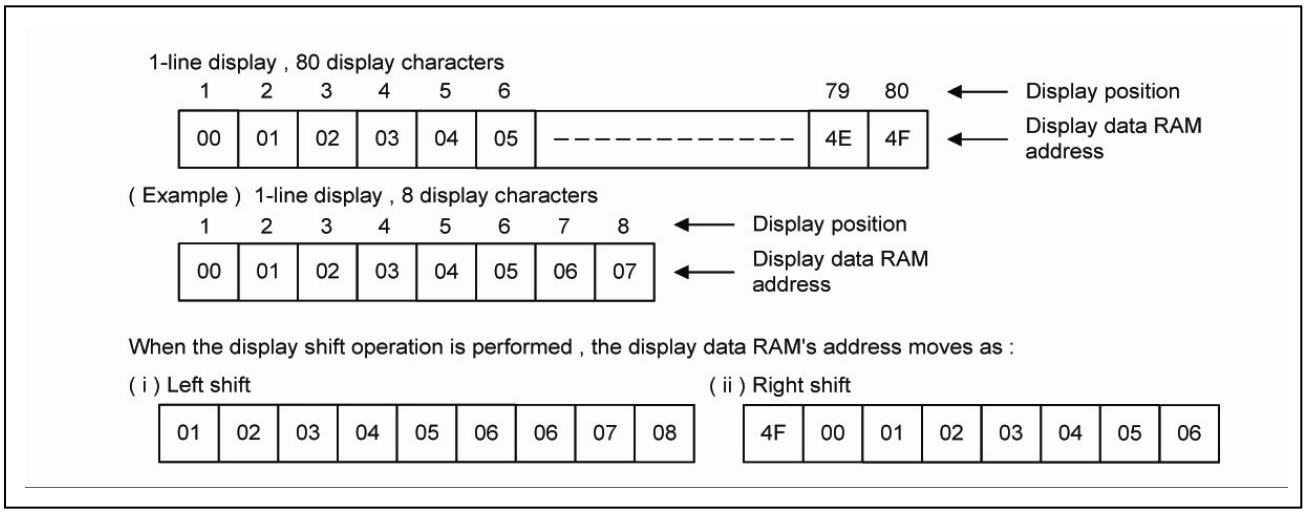


[4-bit Interface]



6.5 Display Data RAM (DD RAM)

The DD RAM stores display data and its RAM size is 80 bytes. The area in DD RAM that is not used for display can be used as a general data RAM. Its address is set in the address counter. There are relations between the display data RAM's address and the LCD's position as shown below.



6.6 Timing Generation circuit

The timing generation circuit generates clock signals for the internal operations

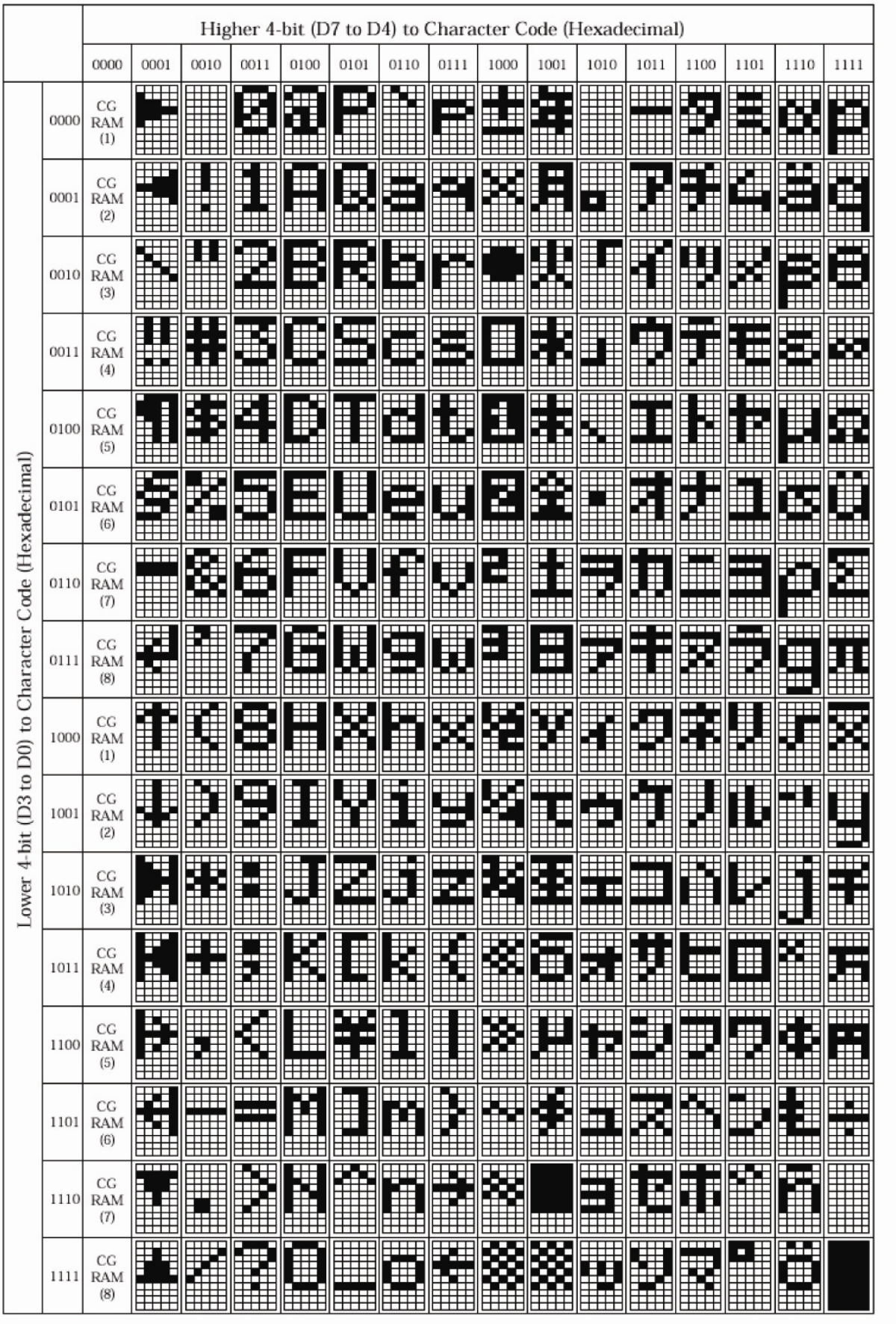
6.7 Character Generator ROM (CG ROM)

CG ROM has a 5 x 7 dots 192 character pattern using 8-bit character code.

6.8 Character Generator RAM (CG RAM)

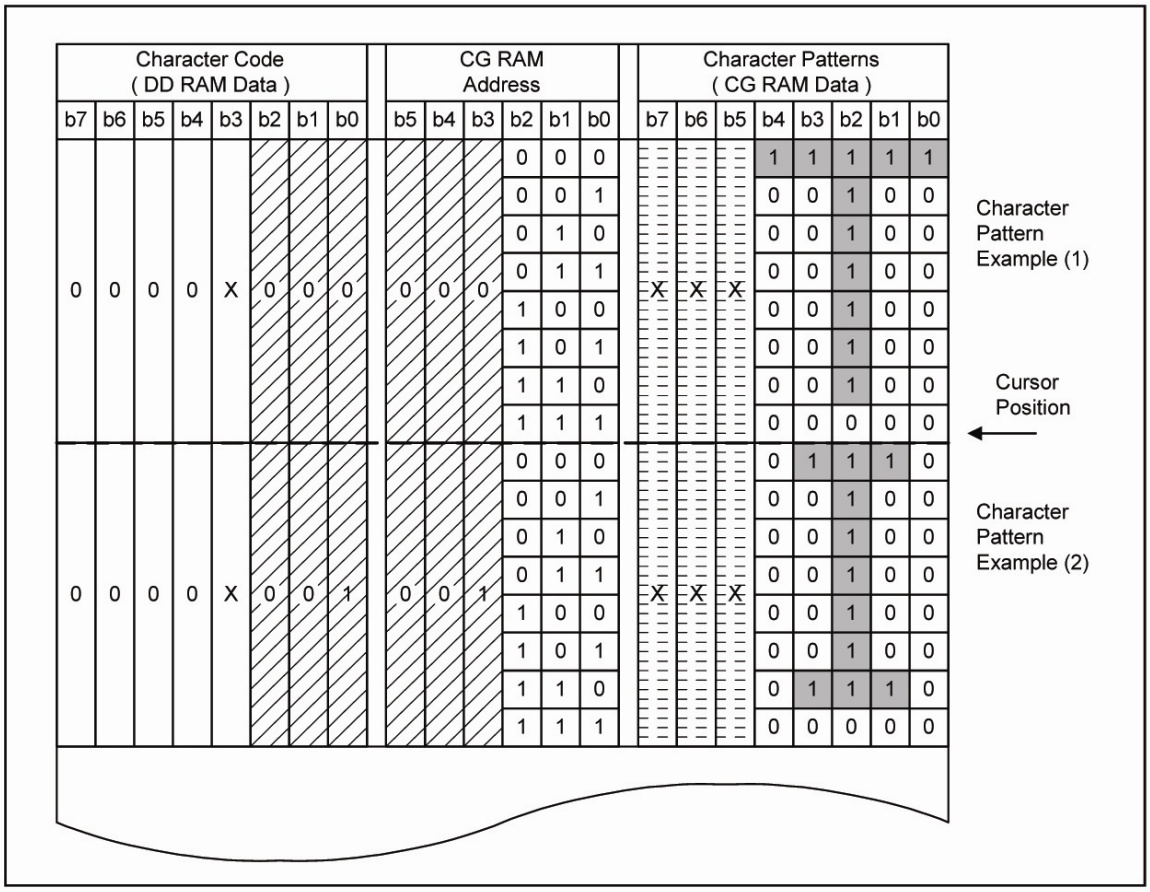
Using the programs, users can easily change the character patterns in the character generator RAM. It can be written with 5 x 8 dots, 8 character patterns.

Correspondence between Character Codes and Character Patterns.



The relations between character generator RAM addresses, character generator RAM data (character patterns) and character codes are shown as below:

6.9 5 x 8 dots character patterns



Note1: ▨ It means that the bits0-2 of the character code corresponds to the bit3-5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be read for the general data RAM.

Note3: When all of the bit4-7 of the character code is 0, CG RAM character patterns are selected.

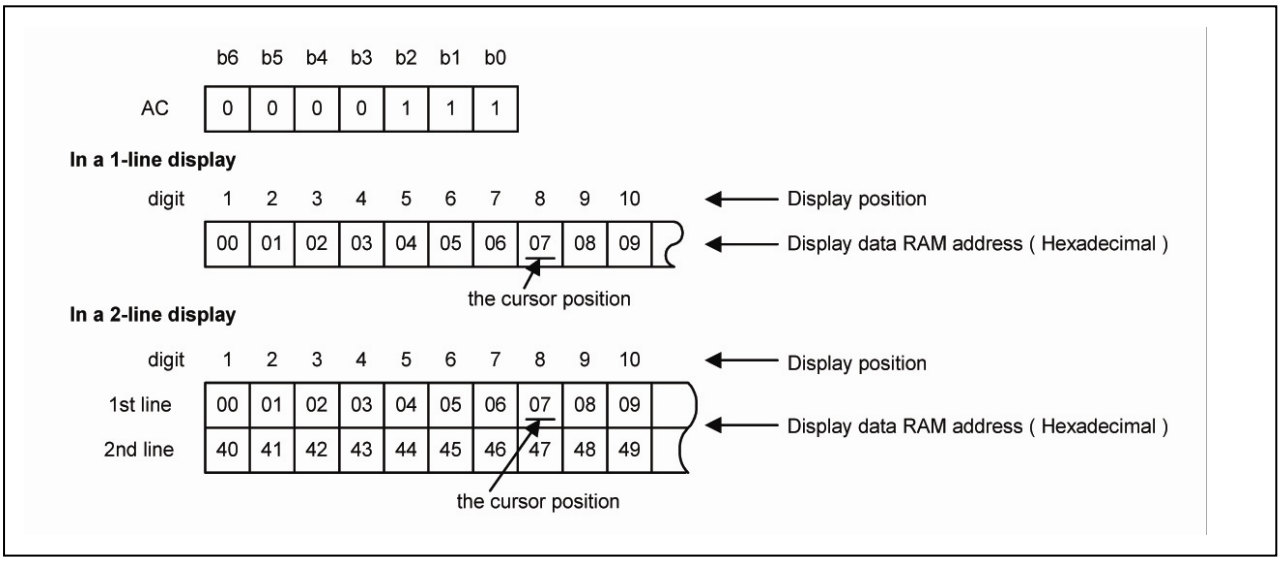
Note4: “1” selected, “0” Not selected, “X”: Don’t Care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7 – b4 = 0) to display “T”. That means character code 00H and 08H can display “T” character.

Note6: The bits 0-2 of the character code RAM is the character pattern line position. The 8^{th} line is the cursor position and display is formed by logical OR with the cursor.

6.10 Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter. When the address counter is $(07)_{16}$, the cursor's position is shown as follows:



6.11 Interfacing to MPU

There are two types of data operations: 4-bit operation and 8-bit operation. Using 4-bit MPU, the interfacing 4-bit data is transferred through DB7 – DB4. The bus lines of DB0 – DB3 are not used. Using 4-bit MPU to transmit an 8-bit data needs two 4-bit data transmissions. First, the higher 4-bit data (DB7 – DB4) is transferred by 4-bit bus line. Secondly, the lower 4-bit (DB3 – DB0) is transferred by 4-bit bus line. Using 8-bit MPU, an 8-bit data is transferred by 8-bit bus lines (DB0 – DB7).

6.12 Register – IR (Instruction Register) and DR (Data Register)

MLCM8016 has two 8-bit registers – IR (instruction register) and DR (data register). In the following, we can use combinations of the RS pin and the R/W pin to select the IR and DR.

RS	R/W	Operation
0	0	IR Write(Display clear, etc)
0	1	Read busy flag (DB7) and address counter (DB0 – DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

6.13 Busy Flag (BF)

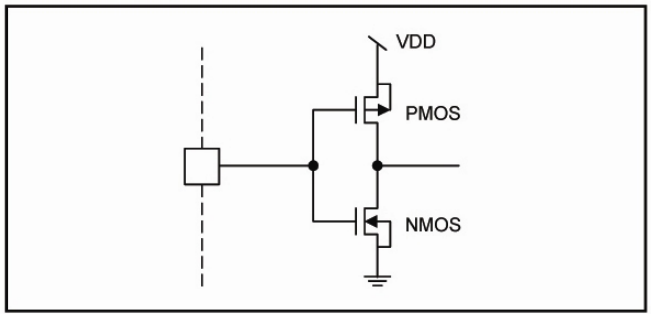
When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag = 1, MLCM8016 is in busy state and does not accept any instructions until the busy flag = 0.

6.14 Address Counter (AC)

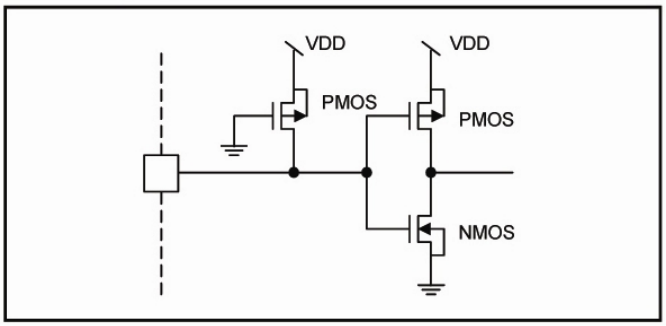
The address counter assigns addresses to display data RAM and character generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing into (or reading from) display data RAM or character generator RAM, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB0 – DB6 when RS = 0 and R/W = 1.

6.15 I/O port configuration

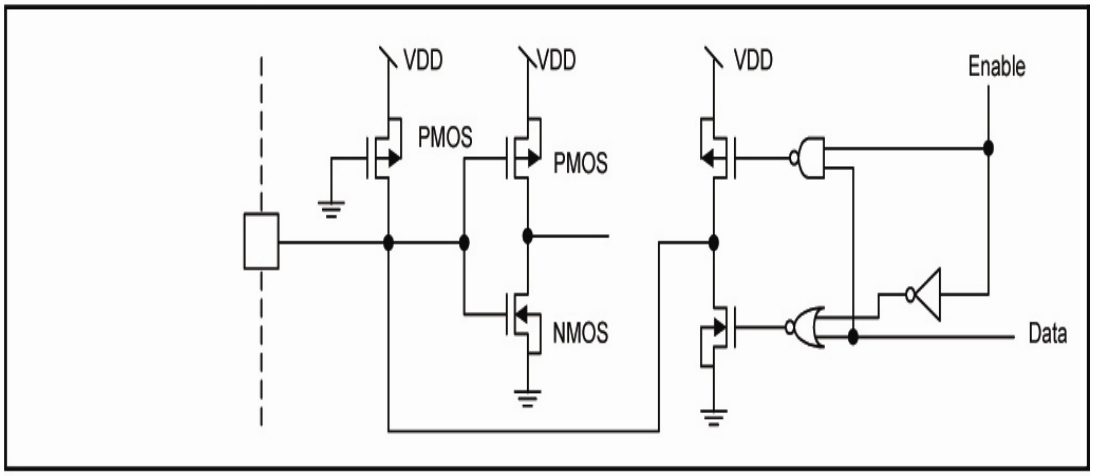
6.15.1 Input port: E



6.15.2 Input port: R/W, RS



6.15.3 Input / Output port: DB0 – DB7



7. Electrical Specifications

7.1 Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{pp}	VDD-0.3V to VDD+7.0V
Input Voltage Range	V_{IN}	-0.3V to VDD+0.3V
Operating Temperature	T_A	-20℃ to +70℃
Storage Temperature	T_{STO}	-30℃ to +80℃

Note: Stresses beyond those given in the Absolute Maximum Rating may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2 DC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	4.5	-	5.5	V	
Operating Current	I_{DD}	-	0.8	1.0	mA	Internal clock (Note)
Input High Voltage	V_{IH1}	2.2	-	VDD	V	Pins: (E, RS, R/W, DB0 – DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Current	I_{IH}	-	-	2.0	uA	Pins: (E, RS, R/W, DB0 – DB7) VDD = 5.0V
Input Low Current	I_{IL}	-30	-80	-125	uA	
Output High Voltage (TTL)	V_{OH1}	2.4	-	VDD	V	I_{OH} = -0.1mA, Pins: DB0 – DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA, Pins: DB0 – DB7
LCD Voltage	V_{PP}	4.8	-	5.2	V	1/4 bias or 1/5 bias

7.3 AC characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

7.3.1 Internal clock operation

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

7.3.2 LCD bias resistor

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 – R5	3.0	5.0	7.0	K-ohm

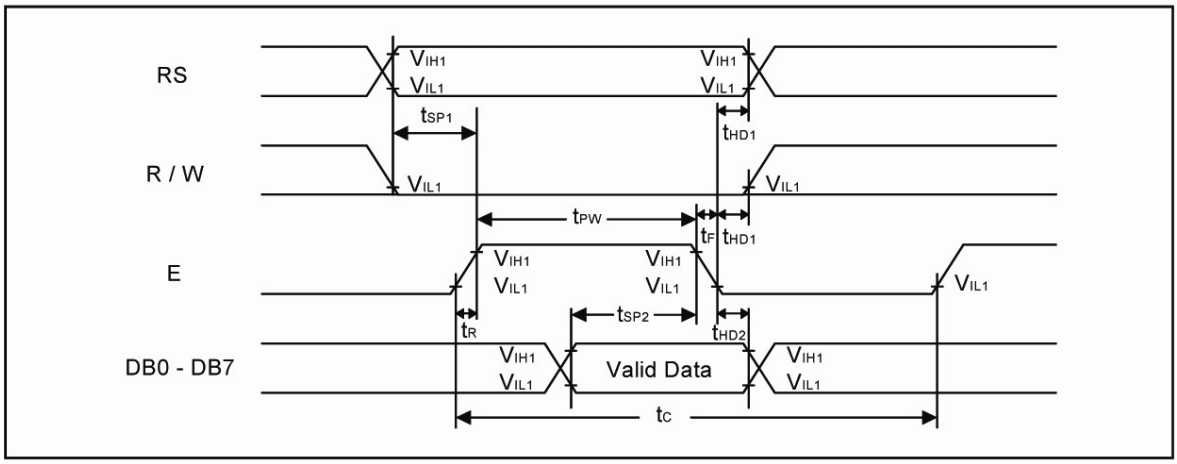
7.3.3 Write mode (writing data from MPU to MLCM8016)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins RS, R/W, E
Data Setup Time	t_{SP2}	80	-	-	ns	Pins: DB0 – DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 – DB7

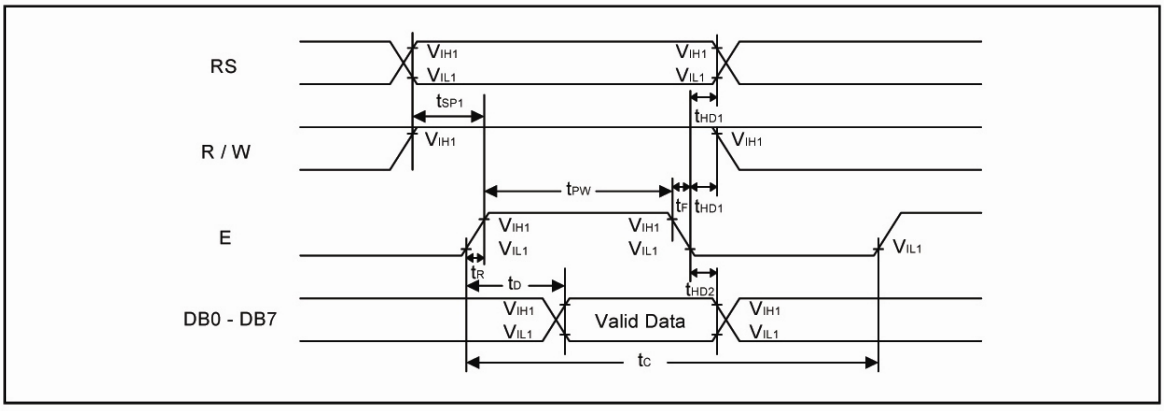
7.3.4 Read mode (reading data from MLCM8016 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins RS, R/W, E
Data Output Delay Time	t_D	-	-	160	ns	Pins: DB0 – DB7
Data Hold Time	t_{HD2}	5	-	-	ns	Pins: DB0 – DB7

7.4 Write mode timing diagram (Writing data from MPU to MLCM8016)



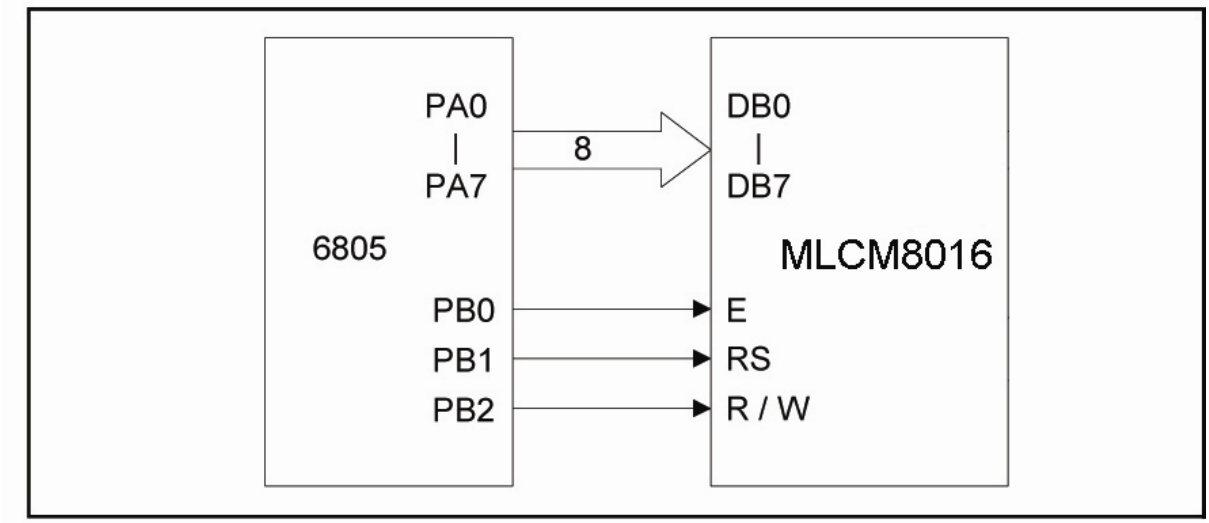
7.5 Read mode timing diagram (Reading data from MLCM8016 to MPU)



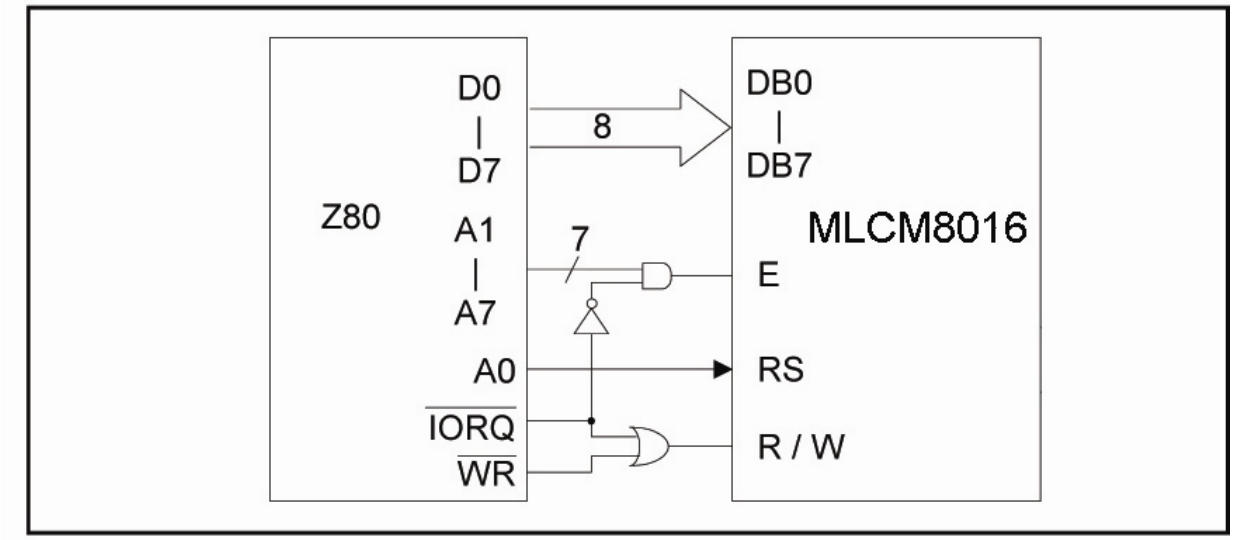
8. Application Circuit

8.1 Interface to MPU

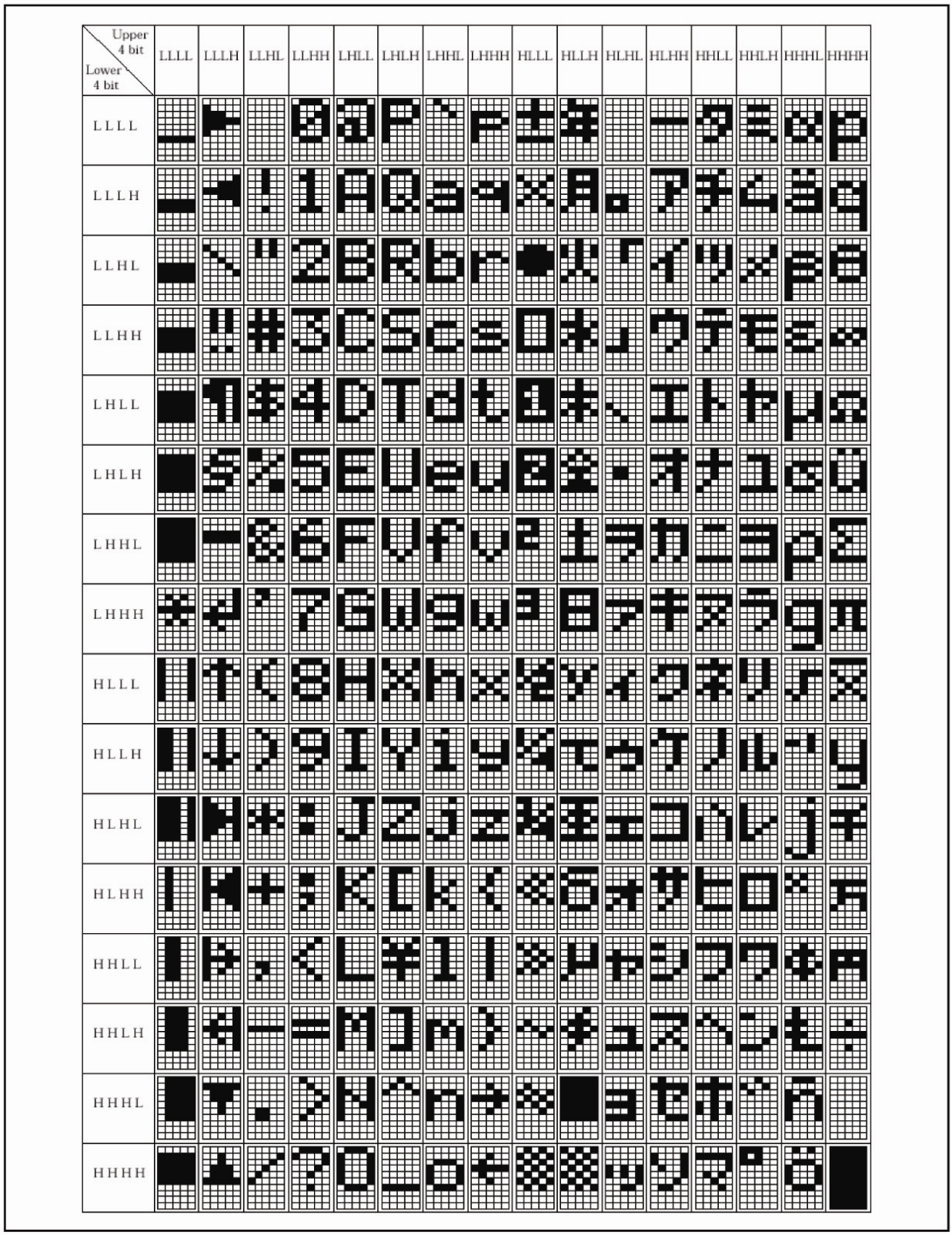
8.1.1 Interface to 8-bit MPU (6805)



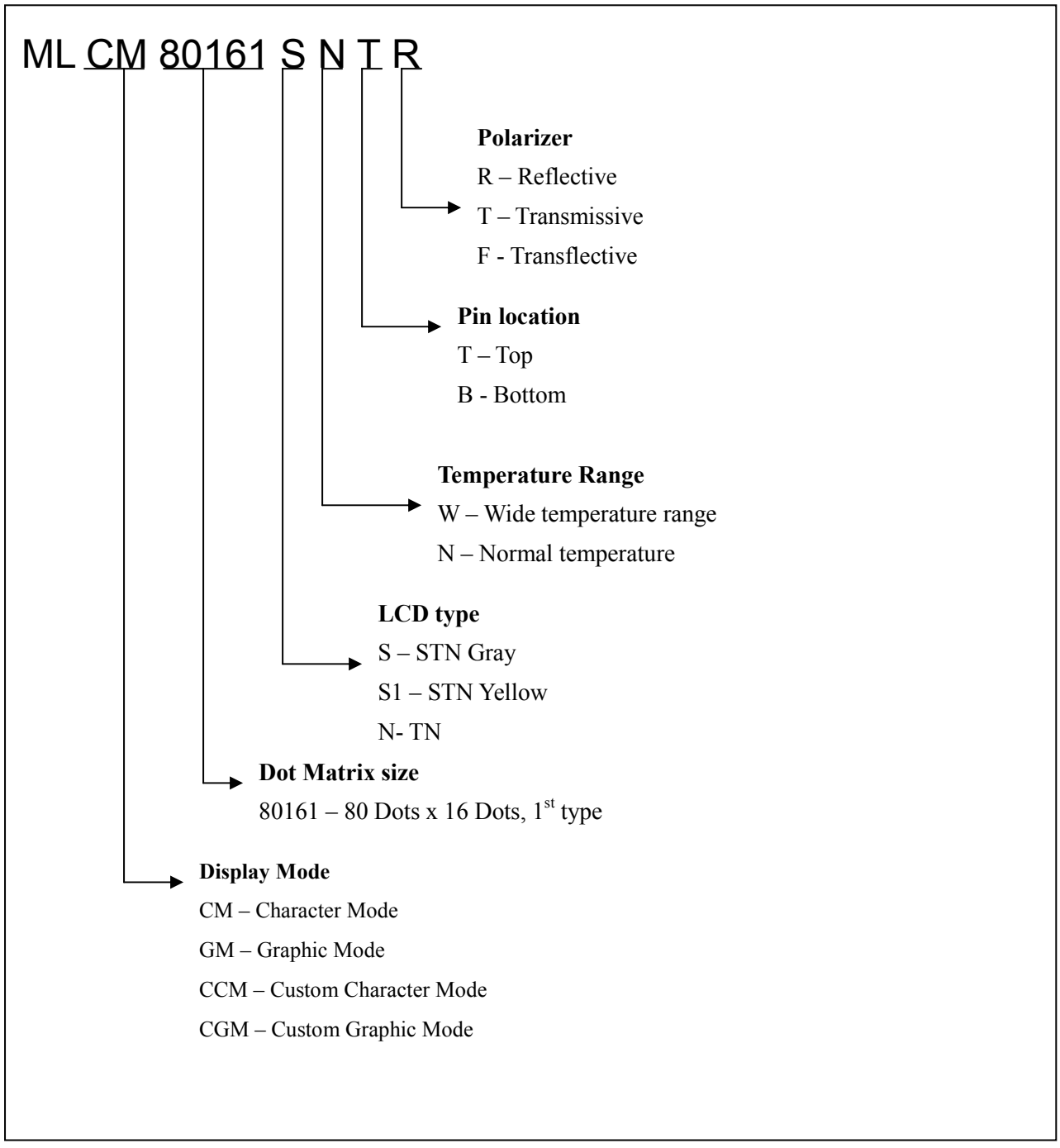
8.1.2 Interface to 8-bit MPU (Z80)



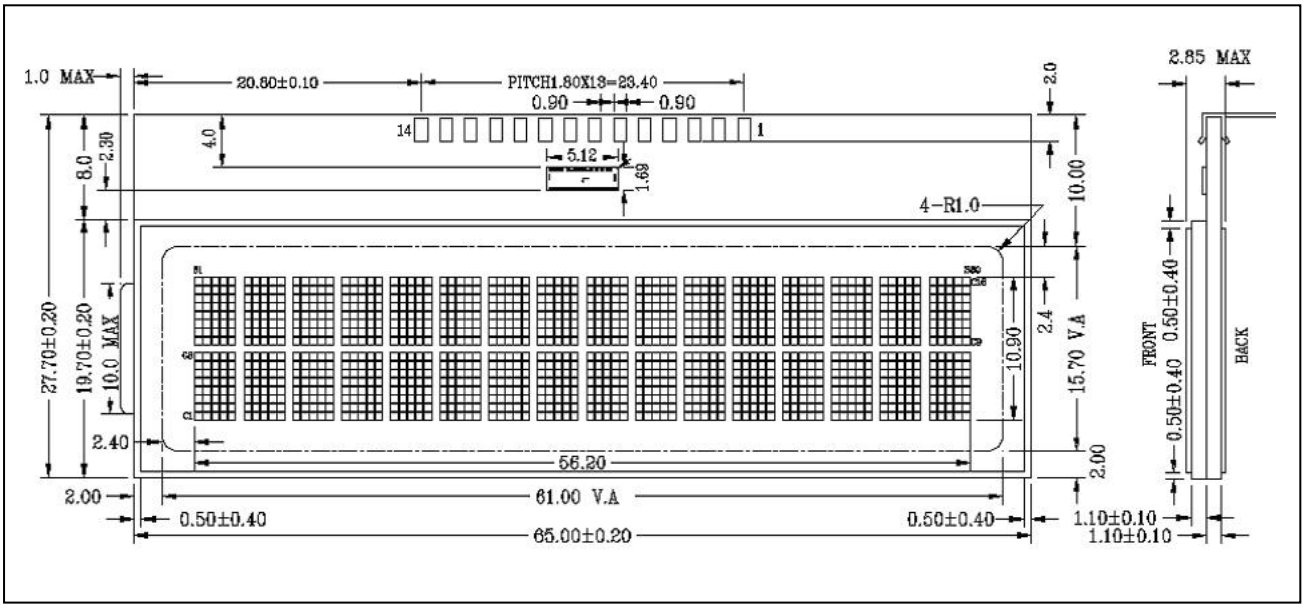
9. Character generator ROM



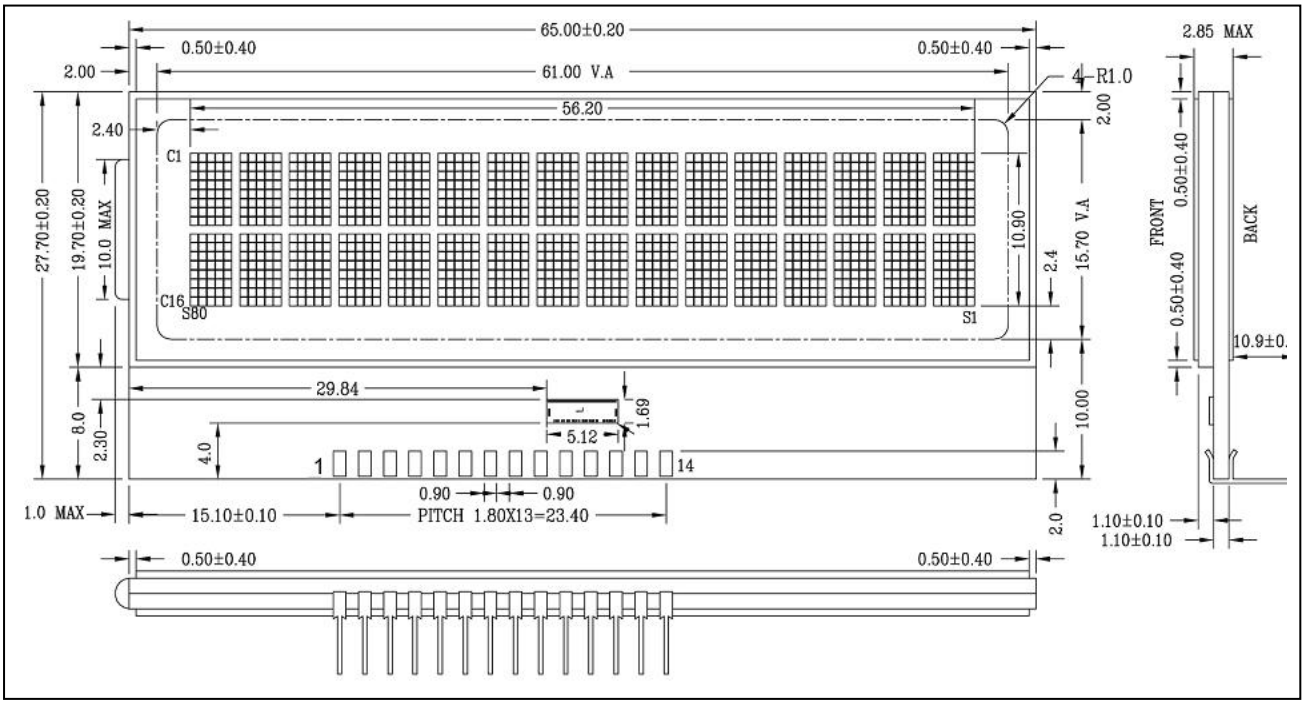
10. LCM ordering information



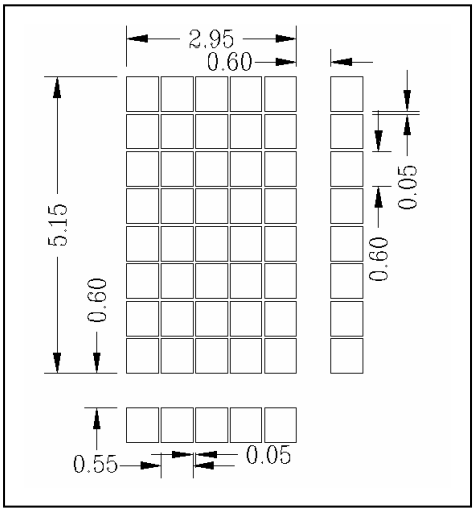
11. MLCM80161SNT Mechanical Dimension



12. MLCM80161SNB Mechanical Dimension



13. MLCM80161SN Dot Dimension



14. MLCM8016SN Pin Assignment

Pin No	Symbol	Type	Level	Function
1 - 4	DB7 – DB4	I/O	H/L	High-order 4 data bits
5 - 8	DB3 – DB0	I/O	H/L	Low-order 4 data bits
9	E	I	L->H	Start signal to read or write data
10	R/W	I	H/L	Select Read or Write. H : Read L : Write
11	RS	I	H/L	Select Register H : Data register (for read and write) L : Instruction Register (for write)
12	VPP	I	-	LCD voltage; either connected to VDD or external variable resistor to adjust contrast
13	VDD	I	-	Power Supply; 4.8V to 5.2V
14	GND	I	-	Ground